In the Claims:

Please cancel claims 9-16 and 31-34.

The claims are as follows:

1-16 (Canceled)

17. (Previously presented) A clock and data recovery circuit comprising:

means for generating a first and a second clock signal;

a first phase adjustment circuit that receives said first clock signal and that generates a third clock signal from said first clock signal and a second phase adjustment circuit that receives said second clock signal and that generates a fourth clock signal, wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively;

means for receiving said third and fourth clock signals and a serial data stream and for generating a reconstructed serial data stream and a phase error signal;

means for receiving said phase error signal and for generating a phase adjustment signal and means for receiving said phase adjustment signal by said means for generating a first and a second clock signal in a feedback loop to adjust the phases of said first and second clock signals.

18. (Previously presented) The circuit of claim 17, further including means for receiving said third clock signal and said reconstructed serial data stream and for generating a parallel data stream.

19. (Original) The circuit of claim 17, wherein the phase of said third clock signal is adjustable in a phase range centered on the high/low transition of said serial data stream.

20. (Previously presented) The circuit of claim 19, wherein the amount of phase adjustment of said third clock signal is a function of the magnitude and polarity of a control voltage applied to said first phase adjustment circuit.

21. (Original) The circuit of claim 17, wherein the phase of said third clock signal is aligned to the zero transition of said serial data stream.

22. (Original) The circuit of claim 17, wherein the phase of said fourth clock signal is adjustable in a phase range centered on the zero transition of said serial data stream.

23. (Previously presented) The circuit of claim 19, wherein the amount of phase adjustment of said fourth clock signal is a function of the magnitude and polarity of a control voltage applied to said second phase adjustment circuit.

24. (Original) The circuit of claim 17, wherein the phases of said first and second clock signals are 90 degrees apart.

25. (Original) The circuit of claim 17, wherein the phase of said third clock signal differs in a phase range of +/- 90 degrees from the phase of said first clock signal and the phases of the second clock signal and fourth clock signals are the same.

26. (Original) The circuit of claim 25, wherein the center of the phase range of said third clock signal is offset +/-90 degrees from the phase of said fourth clock signal.

27. (Previously presented) The circuit of claim 25, wherein the phase difference between said first clock signal and said third clock signal is a function of the magnitude and polarity of a control voltage applied to said first phase adjustment circuit.

28. (Original) The circuit of claim 17, wherein the phase of said third clock signal differs in a phase range of +/- 90 degrees from the phase of said first clock signal and the phase of said fourth clock signal differs in a phase range of +/- 90 degrees from the phase of said second clock signal.

29. (Original) The circuit of claim 28, wherein the center of the phase range of said third clock signal is offset +/-90 degrees from the center of the phase range of said fourth clock signal.

30. (Previously presented) The circuit of claim 28, wherein an amount of phase difference between said first and third clock signals is the same as an amount of phase difference between said second and fourth clock signals and is a function of the magnitude and polarity of a control voltage applied to both said first and second phase adjustment circuits.

31-34 (Canceled)

35. (Previously presented) The circuit of claim 17, wherein said means for generating said first and second clock signals comprises an oscillator.

36. (Previously presented) The circuit of claim 17, wherein the amount of phase adjustment of said third clock signal is a function of the magnitude and polarity of a first control signal applied to said first phase adjustment circuit and wherein the amount of phase adjustment of said fourth clock signal is a function of the magnitude and polarity of a second control signal applied to said second phase adjustment circuit.

37. (Previously presented) The circuit of claim 36, wherein first and second control signal are differential voltage signals.

38. (Previously presented) The circuit of claim 36, wherein said first and second control signals are the same control signal.

39. (Previously presented) A clock and data recovery circuit, comprising:

a clock generation circuit that generates a first and a second clock signal and that receives a feedback signal;

a first phase adjustment circuit that receives said first and second clock signals and a first control signal and that generates a third clock signal;

a second phase adjustment circuit that receives said first and second clock signals and a second control signal and that generates a fourth clock signal;

a phase detector and data recovery circuit that receives said third and fourth clock signals and an input data stream and that generates a reconstructed data stream and a phase error signal;

a proportional/integral circuit that receives said phase error signal and generates said feedback signal; and

a de-multiplexer that receives said third clock signal and said reconstructed data stream and that generates an output data stream.

40. (Previously presented) The circuit of claim 39, wherein said first and second control signals are the same signal.

41. (Previously presented) The circuit of claim 39, wherein said first, second, third and fourth clock signals and said first and second control signal are differential voltage signals.

42. (Previously presented) The circuit of claim 39, wherein said first, second, third and fourth clock signals and said first signal are differential voltage signals and said second control signal is a single voltage level signal.

43. (Previously presented) The circuit of claim 39, wherein said input data stream is a serial data stream and said output data stream is a parallel data stream.

44. (Previously presented) The circuit of claim 39 wherein the phases of said first and second clocks are 90 degrees apart.